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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,573	07/27/2001	Thomas Marra	262/090	1029

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09-917,573	Applicant(s) Marra et al.
	Examiner SHINGLETON	Group Art Unit 2817

—The MAILING DATE of this communication appears on th cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 12-24-2002.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-20 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Atta hment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 7

☐ Int rview Summary, PTO-413

☐ Notice of Ref rence(s) Cited, PTO-892

☐ Notice of Informal Pat nt Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing R view, PTO-948

☒ Other _____

Office Action Summary

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mattila et al. 5,432,473 (Mattila) of record.

Figure 2 of Mattila discloses a biasing circuit for biasing a device used for amplifying a radio frequency (RF) signal (See abstract and column 3), the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, the biasing circuit having an active element operational amplifier configured as a inverting amplifier N21 having an input and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth and a resistor R31 having an input connected to the active element output, wherein a direct current (DC) bias voltage applied at the active element input produces a fixed DC voltage at the resistor input (See column 4, lines 41-48). Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made.

Claims 5-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattila et al. in view of Rubin et al. 4,320,352 (Rubin).

Figures 1 and 2 of Mattila disclose an amplifier circuit for amplifying a radio frequency (RF) signal (See abstract and column 3), the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, having a direct current (DC) bias voltage source (Vref and Vpwr), a biasing circuit (Figure 2), the biasing circuit having an active element operational amplifier configured as

a inverting amplifier N21 having an input connected to the DC bias voltage source and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth of the RIF signal and a resistor R31 having an input connected to the active element output and an output connected to the power amplifier, such that the DC bias voltage source provides a fixed DC voltage at the resistor input, regardless of voltage fluctuations of the RF signal received at the power amplifier. Alternatively, the selection of the bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made. Mattila is silent on the power amplifiers 3 having a transistor with an input for receiving the RF signal. Mattila does show generic conventional elements for the power amplifiers.

Rubin discloses a conventional GaAs FET used for large signal operations (See column 2, line 32) thereby forming a power amplifier for RF applications (See column 1, lines 9 and 10).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a GaAs FET power amplifier for the power amplifier units of Mattila because, as the reference is silent as to the construction of the power amplifiers, any art-recognized equivalent power amplifier would have been usable such as the conventional GaAs FET power amplifier of Rubin wherein the input is applied as the gate thereof.

With respect to claims 13-20, Figures 1 and 2 of Mattila disclose a wireless communication device (See cellular telephone use recited in column 3) having an amplifier circuit (Figure 1) for amplifying a radio frequency (RF) signal, the RF signal comprising an amplitude modulated carrier having an amplitude modulation bandwidth, the amplifier circuit having a direct current (DC) bias voltage source (Vref and Vpwr), a biasing circuit (Figure 2), the biasing circuit having an active element operational amplifier configured as a inverting amplifier N21 having an input connected to the DC bias voltage source and an output, wherein during its operation, i.e. during low and large signal inputs, due to the driver circuits like Q30 the active element inherently maintains a relatively low output impedance over a bandwidth comparable to the amplitude modulation bandwidth of the RIF signal and a resistor R31 having an input connected to the active element output and an output connected to the power amplifier, such that the DC bias voltage source provides a fixed DC voltage at the resistor input, regardless of voltage fluctuations of the RF signal received at the power amplifier. Alternatively, the selection of the

bandwidth and the resistance value of the driver like Q30 so as to keep the operational amplifier N21 from saturating and thus keeping the output impedance thereof low is merely the selection of the optimum or workable range and as this involves routine skill in the art the selection of the bandwidth and resistance of the driver would have been obvious to one of ordinary skill in the art at the time the invention was made. Mattila is silent on the power amplifiers 3 having a transistor with an input for receiving the RF signal. Mattila does show generic conventional elements for the power amplifiers.

Rubin discloses a conventional GaAs FET used for large signal operations (See column 2, line 32) thereby forming a power amplifier for RF applications (See column 1, lines 9 and 10).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted a GaAs FET power amplifier for the power amplifier units of Mattila because, as the reference is silent as to the construction of the power amplifiers, any art-recognized equivalent power amplifier would have been usable such as the conventional GaAs FET power amplifier of Rubin. Note that the biasing circuit of Mattila combined with the GaAs FET of Rubin also forms "A gate bias circuit for biasing a gate of a field effect transistor..." as recited in claim 18.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:30 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
March 22, 2003

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817